REMARKS

Claims 1-18 are pending in this application. Claims 1-18 stand rejected. By this Amendment, claim 2 has been amended. The amendment made to claim 2 does not alter the scope of this claim, nor has this amendment been made to define over the prior art. Rather, the amendment to claim 2 has been made to correct a typographical error. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

Paragraph 4 of the Office Action rejects claims 1-18 under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. The Office Action asserts that the claims contain subject matter not described in the specification. Applicants respectfully request reconsideration and withdrawal of this rejection.

The Office Action asserts that the specification does not provide support for the limitation "a memory bus that accesses said memory; a memory access width controller that controls said quantization controller such that bit allocation is controlled in relation to a number of bits of the memory bus that access said memory" as shown in Claim 1. The Office Action objects to similar recitations in the remaining claims.

In Applicants' previous amendment, the term "memory access unit" was replaced with the term "memory bus that accesses said memory". Further, in claim

1, the memory bus that accesses said memory was explicitly claimed rather than being inferentially claimed as it was originally.

Applicants assert that the term "memory bus" is equivalent to the memory access unit and is merely a more generally accepted term for the same. The term "memory access unit" is nothing more than the data bus which accesses the memory. See page 5, line 25 (*et seq.*) Applicants are merely being their own lexicographer in utilizing the term "memory bus that accesses said memory," which is, in fact, the generally accepted use of that term which and is the proper use and description of the claimed limitation. In the present specification, the memory access width control section 25 takes account of a compression ratio based on an occupied ratio of the frame memory 22, and applies bit allocation control to the quantization control section 24, which is in conformity with the number of bits of a memory access unit. Page 12, line 17 (*et seq.*) In the present system, the number of bits of a memory access unit is utilized during decompression. Thus, Applicants respectfully request reconsideration and withdrawal of this rejection.

Paragraph 5 of the Office Action objects to claim 2 under 35 U.S.C. § 112, second paragraph. Applicants have amended claim 2 to correct for a typographical error. As such, Applicants respectfully request that the rejection to claim 2 be withdrawn.

Paragraph 7 of the Office Action objects to claims 1-14 and 16-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,208,689 ("Ohira"). Applicants respectfully request reconsideration and withdrawal of this rejection.

To anticipate a claim under 35 U.S.C. § 102, the cited reference must disclose every element of the claim, as arranged in the claim, and in sufficient detail to enable one skilled in the art to make and use the anticipated subject matter. See, PPG Industries, Inc. v. Guardian Industries Corp., 75 F.3d 1558, 1566 (Fed. Cir. 1996); C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1349 (Fed. Cir. 1998). A reference that does not expressly disclose all of the elements of a claimed invention cannot anticipate unless all of the undisclosed elements are inherently present in the reference. See, Continental Can Co. USA v. Monsanto Co., 942 F.2d 1264, 1268 (Fed. Cir. 1991).

Among the limitations of Applicants' claims not shown or disclosed in Ohira is a memory access width controller that controls said quantization controller such that bit allocation is controlled in relation to a number of bits of the memory bus that accesses said memory. Ohira is silent as to this limitation.

The Examiner merely repeats the rejection set forth in the Office Action of September 24, 2003 and the further description of the rejection in the Final Office Action dated March 5, 2004, in which the Examiner asserted that Ohira teaches that the compression rate judging section 106 judges a rate of the decoded data 151 and stored in the frame memory based on the size of the image in connection with the storage capacity of the frame memory. The compression rate judging section 106 selects a compression mode from among the plurality of compression modes based on the rate of compression. However, at no time does Ohira discuss the bus accessing the memory (the memory access unit).

The Examiner further asserted that the Z number of bits within the memory is equivalent to the bus accessing the memory. However, this is incorrect, as the bus accessing the memory can be any number of bits wide regardless of the width of the actual memory. Applicants respectfully submit that Ohira fails to consider the number of bits of the memory bus that accesses the memory in performing a decoding operation. Thus, Ohira fails to disclose Applicants' invention.

As can be seen from the components of the Ohira reference, one difference between the present invention and Ohira is the claimed memory access width controller and Ohira's compression rate judging section 106, shown in Figure 18. The present invention utilizes the number of bits of the memory bus width accessing the memory, whereas the cited Ohira reference is an operation relating to the compression rate for compressing the image data. The statement at column 13, lines 8-28 does not teach the present invention.

The Office Action argues that "the compression rate judging section 106" judges a rate of the decoded date 151 to be compressed and stored in the frame memory based upon the size of the image in connection with the storage capacity of the frame memory" discloses the present invention. Applicants disagree with this interpretation of Ohira. Ohira states that the compression rate is decided with the storage capacity and the image size.[1] The storage capacity is discussed at column

[1] The compression judging rate section providing the rate of compression in connection with the storage capacity of the frame memory 103 utilizes the expression T x U x R/LM £ Z with Z being the number of bits within memory 103

13, line 20. The statement "the predictive/display frame memory section 103 including claim memory, being assigned a predetermined storage capacity stores image data on a frame basis" exists therein. This merely means that the image data is stored in a predetermined storage capacity on a frame basis.

Applicants further disagree that the number of bits of the memory access unit is included in the concept of storage capacity. The mere mention of storage capacity for storing the image refers to, for example, the size of the data that can be written in the memory. As such, Applicants assert that the unit for writing the data is included therein, i.e., the memory bus accessing the memory. For example, there are various memories having the same capacity of 128 megabytes of which the data bus width (equivalent to the number of bits of a memory access unit) is 8 bits, 16 bits, 32 bits, etc. In a case where the teaching of Ohira is used, the compression data rate is not altered, even though the memory having a different data bus width is employed. On the other hand, where the claimed invention is used, when the memory having a different data bus is employed, the data compression rate is altered.

In other words, according to Applicants' explicitly recited claim, in the present invention, not only the storage capacity and the size of the image affect the compression rate but also the number of bits of a memory access unit specific to the memory. In contrast, in the Ohira reference, a predetermined storage capacity

---

and LM being the rate of compression. Z represents the size of the memory, not the width of the data bus accessing the memory.

storage image stores image data on a frame basis. As such, the Ohira reference fails to disclose Applicants' explicitly recited claims.

Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: October 20, 2004

Respectfully submitted,

By_____
Ian R. Blum
Registration No.: 42,336
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 Avenue of the Americas
New York, New York 10036-2714
(212) 835-1400
Attorney for Applicant

IRB/mgs